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1 Scope of Document

This document specifies requirements on the module RAM Test.

This document covers requirements only for software algorithms to check the RAM. A hardware RAM check (like ECC check) is not in the scope of this document.

2 Conventions to be used

2.1 Document Conventions

The representation of requirements in AUTOSAR documents follows the table specified in [TPS_STDT_00078], see [1, Standardization Template].

The verbal forms for the expression of obligation specified in [TPS_STDT_00053] shall be used to indicate requirements, see [1, Standardization Template].

The key words “MUST”, “MUST NOT”, “REQUIRED”, “SHALL”, “SHALL NOT”, “SHOULD”, “SHOULD NOT”, “RECOMMENDED”, “MAY”, and “OPTIONAL” in this document are to be interpreted as follows.

Note that the requirement level of the document in which they are used modifies the force of these words.

- MUST: This word, or the adjective “LEGALLY REQUIRED”, means that the definition is an absolute requirement of the specification due to legal issues.
- MUST NOT: This phrase, or the phrase “MUST NOT”, means that the definition is an absolute prohibition of the specification due to legal issues.
- SHALL: This phrase, or the adjective “REQUIRED”, means that the definition is an absolute requirement of the specification.
- SHALL NOT: This phrase means that the definition is an absolute prohibition of the specification.
- SHOULD: This word, or the adjective “RECOMMENDED”, means that there may exist valid reasons in particular circumstances to ignore a particular item, but the full implications must be understood and carefully weighed before choosing a different course.
- SHOULD NOT: This phrase, or the phrase “NOT RECOMMENDED”, means that there may exist valid reasons in particular circumstances when the particular behavior is acceptable or even useful, but the full implications should be understood and the case carefully weighed before implementing any behavior described with this label.
- MAY: This word, or the adjective “OPTIONAL”, means that an item is truly optional. One vendor may choose to include the item because a particular marketplace requires it or because the vendor feels that it enhances the product while another vendor may omit the same item.

An implementation, which does not include a particular option, SHALL be prepared to interoperate with another implementation, which does include the option, though perhaps with reduced functionality. In the same vein an implementation, which does include a particular option, SHALL be prepared to interoperate with another implementation, which does not include the option (except, of course, for the feature the option provides).

2.2 Requirement Structure

Each module specific chapter contains a short functional description of the Basic Software Module. Requirements of the same kind within each chapter are grouped under the following headlines (where applicable):

Functional Requirements:

- Configuration (which elements of the module need to be configurable)
- Initialization
- Normal Operation
- Shutdown Operation
- Fault Operation
- ...

Non-Functional Requirements:

- Timing Requirements
- Resource Usage
- Usability
- Output for other WPs (e.g. Description Templates, Tooling, ...)
- ...

3 Acronyms and abbreviations

The glossary below includes acronyms and abbreviations relevant to RAM Test that are not included in the AUTOSAR Glossary [2].

Abbreviation / Acronym:	Description:
ECU	Electric Control Unit
EOL	End Of Line Often used in the term 'EOL Programming' or 'EOL Configuration'
MAL	Old name of Microcontroller Abstraction Layer (replaced by MCAL because 'MAL' is a french term meaning 'bad')
MCAL	Microcontroller Abstraction Layer
MCU	Microcontroller Unit
NMI	Non maskable interrupt
OS	Operating System
SPAL	The name of this working group
SFR	Special Function Register
RTE	Runtime environment
WP	Work Package
STD	Standard
REQ	Requirement
UNINIT	Uninitialized (= not initialized)

Table 3.1: Acronyms and abbreviations used in the scope of this Document

4 Requirements Specification

This chapter describes all requirements driving the work to define the RAM Test.

4.1 Functional Overview

This module has the task to test the RAM memory area by software.

4.2 Functional Requirements

4.2.1 Configuration

[SRS_RamTst_13800] The number of tested cells shall be changeable at runtime ⌈

Description:	To react on different requirements (sleep, driving cycle) the user shall have the possibility to change the number of tested cells per cycle "online".
Rationale:	Influences the interrupt disable times.
Use Case:	When car is driven the system interrupt locking time must be much shorter than in case of sleep mode.
Dependencies:	–
Supporting Material:	–

⌋

[SRS_RamTst_13801] Test cell size shall be a published parameter ⌈

Description:	The implementer shall chose the test cell size (bit, byte, word, long word) for a specific test implementation according to the controller properties. This parameter shall be published to the integrator along with a specific implementation.
Rationale:	–
Use Case:	Runtime optimization by implementer due to controller properties.
Dependencies:	–
Supporting Material:	–

⌋

[SRS_RamTst_13802] Multiple RAM areas shall be configurable at post build/ link time ⌈

Description:	It shall be possible to configure multiple RAM areas (by configuring their start and end address). If two RAM areas overlap and an error is detected in the overlapping region while testing one of the blocks, the driver does not guarantee to update the status of the other block.
Rationale:	–
Use Case:	User shall have the possibility to configure the memory mapping.
Dependencies:	–
Supporting Material:	–

⌋

[SRS_RamTst_13803] A subset of available RAM Test algorithms shall be selectable at pre-compile time ⌈

Description:	The user shall select at pre-compile time the available algorithms which matches to the project safety requirements.
Rationale:	Avoid unused code.
Use Case:	Depending on ECU safety analysis different RAM test algorithms should be selectable. To save ROM space the algorithms should be selectable at compile time.
Dependencies:	–
Supporting Material:	–

⌋

[SRS_RamTst_13804] A subset of the pre-compile time selected RAM Check test algorithms shall be selectable at runtime ⌈

Description:	The user shall select the test algorithms from those available at runtime to conform to the project safety requirements.
Rationale:	Different levels of testing are available.
Use Case:	During normal operation a simple test is executed and before going to sleep mode a more complex RAM test algorithm will be executed. The complex RAM test can not be executed during normal operation because of stronger interrupt latency requirements.
Dependencies:	[SRS_RamTst_13803]
Supporting Material:	–

⌋

4.2.2 Normal Operation

[SRS_RamTst_13822] A safety mechanism with low coverage shall be available ⌈

Description:	A safety measure which fulfils a diagnostic coverage of 60% shall be available. It may be provided by hardware means, by an appropriate test algorithm, or both.
Rationale:	Detect permanent faults in RAM.
Use Case:	Support of EOL, quick start-up tests and where low diagnostic coverage tests are required, e.g. if system has safety goals with low ISO 26262 ASIL rating only.
Dependencies:	–
Supporting Material:	• [4] Tables 4, 5 and D.1 • [5] Table 33, clause 5.1.13.5 (RAM Pattern test), 5.1.13.6 (Parity bit), 5.1.13.7 (RAM March test)

⌋

[SRS_RamTst_13823] A Test algorithm with medium coverage shall be available ⌈

Description:	A safety measure which fulfils a diagnostic coverage of 90 % shall be available. It may be provided by hardware means, by an appropriate test algorithm, or both.
Rationale:	Detect permanent faults in RAM.
Use Case:	Support of EOL, start-up tests and where medium diagnostic coverage tests are required, e.g. if the latent fault metric of ISO 26262 for the ASIL level of the safety goals of a system can be achieved with medium coverage.
Dependencies:	–
Supporting Material:	• [4] Tables 4, 5 and D.1 • [5] Table 33, clause 5.1.13.5 (RAM Pattern test), 5.1.13.6 (Parity bit), 5.1.13.7 (RAM March test)

⌋

[SRS_RamTst_13824] A Test algorithm with high coverage shall be available ⌈

Description:	A safety measure which fulfils a diagnostic coverage of 99 % shall be available. It may be provided by hardware means, by an appropriate test algorithm, or both.
Rationale:	Detect permanent faults in RAM.
Use Case:	Support of EOL, diligent start-up, shut-down or runtime tests and where high diagnostic coverage tests are required, e.g. if system has a safety goal with high ISO 26262 ASIL rating.
Dependencies:	–

▽

△

Supporting Material:	• [4] Tables 4, 5 and D.1 • [5] Table 33, clause 5.1.13.5 (RAM Pattern test), 5.1.13.6 (Parity bit), 5.1.13.7 (RAM March test)

⌋

[SRS_RamTst_13809] It shall be possible to divide the RAM test execution into smaller pieces ⌈

Description:	It shall be possible to divide the RAM test execution into smaller pieces. With one call of the RAM test it shall be possible to execute only a part of the whole RAM test.
Rationale:	Avoid long interrupt disable times
Use Case:	Drivers who need short interrupt latency times
Dependencies:	–
Supporting Material:	–

⌋

[SRS_RamTst_13810] Current status of RAM test execution per block shall be available through a get status interface ⌈

Description:	RAM test execution status per block (`RESULT_NOT_TESTED`, `RESULT_OK`, `RESULT_NOT_OK`, and `RESULT_UNDEFINED`) shall be provided to the user. User shall have the possibility to get the status of the RAM test at any time. This shall be implemented as a get status interface and shall be configurable during compile time. This function shall be optional.
Rationale:	–
Use Case:	Diagnostics may need to know if there has been errors occurred or not.
Dependencies:	–
Supporting Material:	–

⌋

[SRS_RamTst_13820] RAM test execution status shall be provided by a notification mechanism ⌈

Description:	Information when error has been detected or test has been finished shall be provided to the user by a notification mechanism. This function shall be optional.
Rationale:	–
Use Case:	Diagnostics may need to know immediately if an error has been detected or not.
Dependencies:	–
Supporting Material:	–

⌋

[SRS_RamTst_13811] The RAM test module shall be able to perform its tests in a non-destructive manner ⌈

Description:	The RAM test module shall be able to perform its tests in a non-destructive manner.
Rationale:	Original data shall be preserved.
Use Case:	Destroying of all RAM data may lead to longer reaction times (e.g. wake up), higher resource consumption (e.g.: EEPROM).
Dependencies:	–
Supporting Material:	–

⌋

[SRS_RamTst_13812] The RAM test module shall be able to perform its tests in a destructive manner ⌈

Description:	The RAM test module shall be able to perform its tests in a destructive manner. The state of the RAM after testing shall be defined.
Rationale:	Original data does not need to be preserved.
Use Case:	–
Dependencies:	–
Supporting Material:	–

⌋

4.3 Non-Functional Requirements (Qualities)

[SRS_RamTst_13816] Effects of Instruction / Data queue shall be taken into account ⌈

Description:	When writing to a cell and after reading back this may lead to the problem that the read-back value comes from the data queue and not from the RAM cell to be tested. In that case instruction(s) have to be injected to eliminate such an effect.
Rationale:	Read back the value from a tested cell.
Use Case:	Controller with instruction or data queue may have such effects.
Dependencies:	–
Supporting Material:	–

⌋

[SRS_RamTst_13825] The RAM Test Module shall be usable to comply with requirements of the different ASIL levels of ISO 26262. ⌈

Description:	The RAM Test Module shall provide and document (fault models and fault coverage) diagnostic capability for permanent faults in RAMs to enable fulfillment of the latent fault metric targets of ISO 26262 for the different ASIL levels.
Rationale:	Usability of AUTOSAR for sytems which need to comply with ISO 26262.
Use Case:	–
Dependencies:	–
Supporting Material:	• [4] Tables 4, 5 and D.1 • [5] Table 33, clause 5.1.13.5 (RAM Pattern test), 5.1.13.6 (Parity bit), 5.1.13.7 (RAM March test)

⌋

5 References

[1] Standardization Template
AUTOSAR_FO_TPS_StandardizationTemplate

[2] Glossary
AUTOSAR_FO_TR_Glossary

[3] ISO 26262:2018 Road vehicles -– Functional Safety
https://www.iso.org

[4] ISO 26262-5:2018 Part 5: Product development at the hardware level
https://www.iso.org

[5] ISO 26262-11:2018 Part 11: Guideline on application of ISO 26262 to semiconductors
https://www.iso.org

A Change history of AUTOSAR traceable items

Please note that the lists in this chapter also include traceable items that have been removed from the specification in a later version. These items do not appear as hyperlinks in the document.

A.1 Traceable item history of this document according to AUTOSAR Release R26-11

A.1.1 Added Requirements in R26-11

none

A.1.2 Changed Requirements in R26-11

none

A.1.3 Deleted Requirements in R26-11

none

A.2 Traceable item history of this document according to AUTOSAR Release R25-11

A.2.1 Added Requirements in R25-11

none

A.2.2 Changed Requirements in R25-11

none

A.2.3 Deleted Requirements in R25-11

none

A.3 Traceable item history of this document according to AUTOSAR Release R24-11

A.3.1 Added Requirements in R24-11

Number	Heading
[SRS_RamTst_13800]	The number of tested cells shall be changeable at runtime
[SRS_RamTst_13801]	Test cell size shall be a published parameter
[SRS_RamTst_13802]	Multiple RAM areas shall be configurable at post build/ link time
[SRS_RamTst_13803]	A subset of available RAM Test algorithms shall be selectable at pre-compile time
[SRS_RamTst_13804]	A subset of the pre-compile time selected RAM Check test algorithms shall be selectable at runtime
[SRS_RamTst_13809]	It shall be possible to divide the RAM test execution into smaller pieces
[SRS_RamTst_13810]	Current status of RAM test execution per block shall be available through a get status interface
[SRS_RamTst_13811]	The RAM test module shall be able to perform its tests in a non-destructive manner
[SRS_RamTst_13812]	The RAM test module shall be able to perform its tests in a destructive manner
[SRS_RamTst_13816]	Effects of Instruction / Data queue shall be taken into account
[SRS_RamTst_13820]	RAM test execution status shall be provided by a notification mechanism
[SRS_RamTst_13822]	A safety mechanism with low coverage shall be available
[SRS_RamTst_13823]	A Test algorithm with medium coverage shall be available
[SRS_RamTst_13824]	A Test algorithm with high coverage shall be available
[SRS_RamTst_13825]	The RAM Test Module shall be usable to comply with requirements of the different ASIL levels of ISO 26262.

Table A.1: Added Requirements in R24-11

A.3.2 Changed Requirements in R24-11

none

A.3.3 Deleted Requirements in R24-11

none